High mobility indium free amorphous oxide thin film transistors

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High mobility bottom gate thin film transistors (TFTs) with an amorphous gallium tin zinc oxide (*a*-GSZO) channel layer have been produced by rf magnetron cosputtering using a gallium zinc oxide (GZO) and tin (Sn) targets. The effect of postannealing temperatures (200, 250, and 300 °C) was evaluated and compared with two series of TFTs produced at room temperature (S1) and 150 °C (S2) during the channel deposition. From the results, it was observed that the effect of postannealing is crucial for both series of TFTs either for stability as well as for improving the electrical characteristics. The *a*-GSZO TFTs ($W/L=50/50$ μm) operate in the enhancement mode (*n*-type), present a high saturation mobility of 24.6 cm^2/V s, a subthreshold gate swing voltage of 0.38 V/decade, a turn-on voltage of −0.5 V, a threshold voltage of 4.6 V, and an I_{on}/I_{off} ratio of 8×10^7, satisfying all the requirements to be used as active-matrix backplane. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2937473]

Amorphous oxide semiconductors (AOSs) are becoming one of the most promising semiconductor materials for active-matrix thin film transistor (TFT) based backplane[1] due to the superior electrical performances and better uniformity over large areas, when compared with the conventional amorphous silicon and polycrystalline silicon TFTs, respectively.[2] Several oxide based TFTs have been reported in the last four years with the first ones based on ZnO polycrystalline thin films.[3]

AOSs are very attractive for TFT applications from a manufacturing point of view because they combine simultaneously the advantages of amorphous silicon and polycrystalline silicon based TFTs. They can be produced at room and relatively low temperatures (compatible with low cost polymeric substrates) presenting very smooth surfaces without grain boundaries (advantage for process integration). Based on these results, several reports have been presented with AOS TFTs using different system compositions such as *a*-IZO,[4,5] *a*-GIZO,[6,7] and *a*-ZTO.[8,9] From the TFT analysis, it is clearly observed that in order to achieve high channel mobilities, the most promising candidates are based on systems including In, in percentages higher than 40% for ternary systems. Besides that, since the availability of In is limited (In is a by-product of mining ores for other metals, such as zinc, copper, lead, and tin, as it estimated that <1000 times more zinc (132 ppm) than indium (0.1 ppm) exists in the earth's crust[10]), solutions avoiding the use of In are nowadays preferable.

In this work, we report on the fabrication of high performance oxide TFTs where the In metal cation is substituted by Sn on the semiconductor channel layer.

The TFTs were produced using *p*-type silicon substrates ($N_A\approx10^{17}$ cm^{-3}) coated with 100 nm thick thermally grown SiO_2, which acted as the gate dielectric. Si was simultaneously used as the substrate and the common gate of the devices. A 5/75 nm thick Ti/Au film was deposited by e-beam evaporation on the backside of Si to form the gate electrode. A 50 nm thick *a*-GSZO layer (the semiconductor) was then deposited by rf magnetron cosputtering in a home made sputtering system. A 3 in. diameter $ZnO:Ga_2O_3$ (95:5 wt %) ceramic target and a 2 in. diameter Sn target from super conductor materials (SCM) were used at 15 cm from the substrate, at a base pressure of 3×10^{-4} Pa, an oxygen partial pressure of 1×10^{-1} Pa, a processing pressure ($Ar+O_2$) of 7×10^{-1} Pa and rf power of 75 and 20 W for the $ZnO:Ga_2O_3$ and Sn targets, respectively. The 200 nm thick source/drain electrodes (Ti) were e-beam evaporated on top of *a*-GSZO. Both the semiconductor and the source/drain layers were patterned by lift-off and the produced transistors had a fixed width (W) of 50 μm and length (L) of 50 μm. Two different series of transistors, S1 and S2, were produced. For S1, the *a*-GSZO was produced at room temperature while S2 was deposited at 150 °C. After production, both series of TFTs were annealed in a Barnstead Thermolyne F21130 tubular furnace, in nitrogen, at 150, 200, 250, and 300 °C for 1 h.

The films thicknesses were measured with a surface profilometer Sloan Tech Dektak 3.

X-ray diffraction measurements were performed using the Cu $K\alpha$ line ($\lambda=1.5418$ Å) of a Siemens D-500 diffractometer. The scanning electron microscopy (SEM) analysis was done in a FEI Strata 235-Dual Beam FIB (both in surface and cross section). The atomic force microscopy (AFM) analysis was done with a MFP-3D microscope from Asylum Research in the tapping mode. X-ray photoelectron spectroscopy (XPS) analysis was done using the Al $K\alpha$ (nonmonochromatic) radiation of an XSAM800 (KRATOS) spectrometer operated in the fixed analyzer transmission with a power of 120 W (10 mA and 12 kV).

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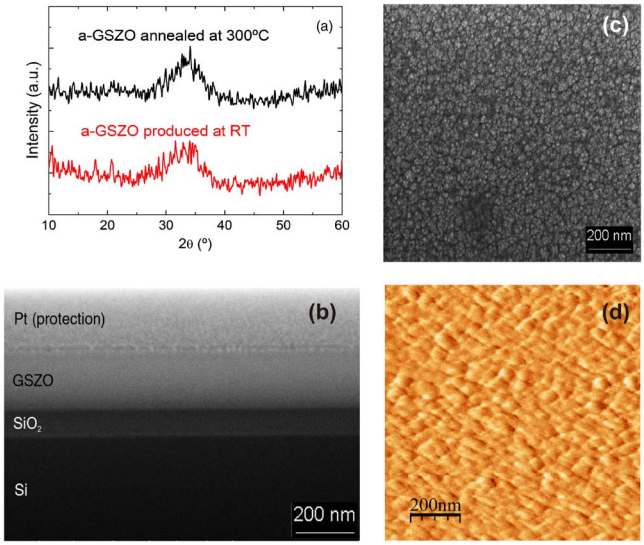

FIG. 1. (Color online) Structural and morphological properties presented by a typical *a*-GSZO film with 175 nm thickness, produced by rf magnetron cosputtering. (a) X-ray diffractogram for *a*-GSZO film deposited at room temperature and annealed at 250 °C. (b) SEM cross section of *a*-GSZO film deposited on SiO_2/c-Si wafer viewed at 52°. (c) Surface morphology by SEM and (d) AFM image, presenting an average roughness around 0.6 nm.

The TFTs were electrically characterized in air at room temperature, in the dark using a Cascade Microtech M150 microprobe station connected to a semiconductor parameter analyzer (Agilent 4155C) controlled by the software METRICS ICS.

Figure 1(a) shows the x-ray diffraction pattern for the *a*-GSZO film used at the channel layer, deposited at room temperature on corning 1737 glass substrate with a thickness of 175 nm (equivalent to S1 series). The two diffractograms refer to the film as produced and post annealed at 300 °C in a N_2 atmosphere, respectively. An amorphouslike behavior is observed which was also confirmed by the SEM cross section of the same film, as shown in Fig. 1(b). The surface morphology is also shown in the SEM image presented in Fig. 1(c). The films present a very smooth surface with an average roughness of 0.6 nm (inferred by AFM analysis).

The results concerning the structural and morphological characterization even after annealing do not present any detectable variation concerning the structure of the films. Nevertheless, the electrical measurements (not presented in this letter) are quite influenced by the annealing temperature. The resistivity for *a*-GSZO (measured with coplanar Al electrodes) as produced is 4.6×10^{10} Ω cm and after annealing decreases about eight orders of magnitude to a value of $\approx1\times10^{2}$ Ω cm, with a Hall mobility (using the van der Pauw configuration) of 5 $cm^2/V\,s$. These results have been also observed by Hosono *et al.*[11] and more recently by Jayaraj *et al.*[12] The decrease in resistivity with increasing annealing temperature is attributed to internal modifications in the semiconductor structure leading to improved local atomic rearrangement, possibly related to a change in the oxidation state of Sn. With increasing annealing temperature, there is a surface enrichment in gallium and, especially in Sn as shown in Table I. Regarding photoelectron BE of different elements, they correspond to the oxidized forms: BE (Ga $2p$) $=1118.7\pm0.2$ eV, typical of Ga $2p$ from Ga_2O_3[13] and BE (Zn $2p$) $=1022.3\pm0.2$ eV typical of Zn $2p$ from ZnO.[14] Concerning Sn, its photoelectrons Sn $3p$ and Sn $3d$ present, in all the samples, binding energies of 716.1 ± 0.2 and 486.2 ± 0.2 eV, respectively, which can be assigned either to SnO or SnO_2 given their binding energy proximity and the dispersion of values in literature. A more robust parameter, independent of charge accumulation correction, is the modified Auger parameter (Sn $M_4N_{45}N_{45}$ kinetic energy+Sn $3d_{5/2}$ BE) which is, for all the samples, 918.3 ± 0.2 eV which is closer to the SnO_2 modified Auger parameter than to the SnO one.[15] O $1s$ peak is fittable with two components centered at 530.4 ± 0.2 and at 532.1 ± 0.2 eV assignable, respectively, to the oxide and hydroxide oxygen forms. The ratio O(oxide)/O(hydroxide) (see Table I) increases with the annealing temperature increase. Another indirect result from XPS data concerns spectra charge shifts which were 9.5, 8.5, and 4 eV for RT, 200 and 300 °C, respectively. This is an indication that the number of hole traps in the samples decrease with the annealing temperature.

Figures 2(a) and 2(b) represent the two series (S1 and S2) of electrical characteristics of *a*-GSZO TFTs at drain-source voltage of 20 V (saturation region), produced at room temperature and 150 °C, respectively, and both postannealed after production at 300 °C. The obtained results are quite similar for the two series of TFTs, presenting S2 slightly improved performance, mainly related to the increase on the saturation mobility to values of the order of 25 $cm^2/V\,s$. In Table II, a comparison of the electrical parameters extracted for the two series of *a*-GSZO TFTs after each annealing temperature stage is presented.

The data reveal a drastic improvement of the electrical properties for both series of *a*-GSZO TFTs. For S1 TFTs, they start to work only for annealing temperatures higher than 250 °C while for S2 TFTs, even though they work after production, the electrical behavior is not stable [for successive and repeated measurements a positive V_{on} shift is observed, which should be related with electron trapping at (or near) the insulator-semiconductor interface]. Only after annealing at 200 °C, the S2 TFTs present stable and reproducible electrical characteristics. Concerning saturation mobility μ_{sat} [calculated by the derivative of the $\sqrt{I_{DS}}(V_{GS})$ plot with $V_{DS}=20$ V] an increase is observed as the annealing temperature increases, for the two series of TFTs analyzed, with a maximum value of the order of 25 $cm^2/V\,s$, for films processed with an initial temperature of 150 °C. This improvement with annealing temperature is attributed to modification

TABLE I. XPS atomic percentages for Zn, Ga, Sn, and O elements and Ga/Zn and Sn/Zn atomic ratios.

Annealing temperature	Ga	Zn	Sn	O (Oxide)	O (Hydroxide)	Ga/Zn	Sn/Zn
RT	1.6	24.6	6.6	35.5	31.7	0.07	0.27
200 °C	1.6	24.6	7.2	40.4	26.2	0.07	0.29
300 °C	2.5	21.2	11.8	45.3	19.2	0.12	0.56

TABLE II. Comparison between the electrical extracted parameters for the two series (S1 and S2) of *a*-GSZO TFTs after each annealing temperature. a) denotes as-deposited, nw denotes not working, and ns denotes not stable.

	S1 (Room temperature)				S2 (150 °C)			
Annealing (°C)	a)	200	250	300	a)	200	250	300
μ_{sat} ($cm^2/V\,s$)	nw	nw	7.9	18.1	ns	10.6	15.4	24.6
V_{th} (V)	nw	nw	6.5	6.5	ns	5.4	4.8	4.6
I_{on}/I_{off}	nw	nw	2×10^7	6×10^7	ns	3×10^8	9×10^8	8×10^7
S (V/decade)	nw	nw	0.75	0.62	ns	0.38	0.46	0.45

of the semiconductor/insulator interface with temperature and/or to improved local atomic rearrangement[8] as it was confirmed by XPS analysis. The threshold voltage V_{th} is almost independent of the initial processing conditions as well as of the annealing temperature, remaining an average value of 5 V. The I_{on}/I_{off} ratio for the S1 series increases by factor of 3 (from 250 to 300 °C), while for S2 series an increase is observed from 200 to 250 °C (from 3×10^8 to 7×10^8) and a decrease for 300 °C (8×10^7). A different behavior is observed for the subthreshold voltage swing (S). For TFTs from series S1, a decrease is observed in S, from 0.75 to 0.62 V/decade, suggesting a better interface when the devices are annealed at higher temperatures. On the other hand, for the TFT from series S2, an opposite dependence is observed, as the annealing temperature increases from 200 to 250 °C. Here, a deterioration of the S value is observed, from 0.38 to 0.45 V/decade, followed by stabilization at 300 °C.

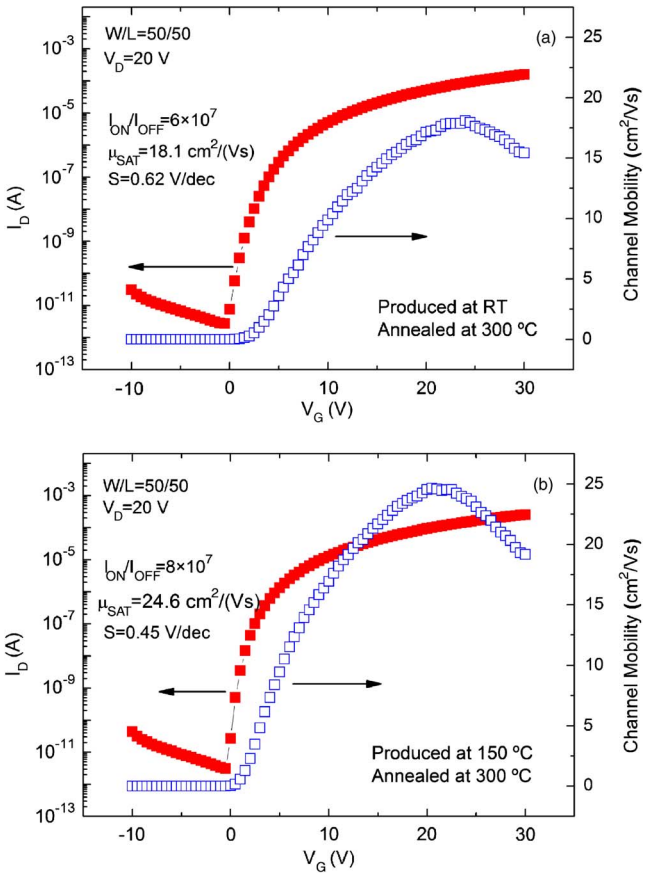

FIG. 2. (Color online) I_D-V_G transfer characteristics obtained at V_D=20 V (saturation region) for *a*-GSZO TFT produced at (a) room temperature (S1) and (b) produced at 150 °C (S2). Both devices were postannealed at 300 °C in a nitrogen atmosphere for 1 h. The saturation mobility μ_{sat} was calculated by the derivative of the $\sqrt{I_{DS}}(V_{GS})$ plot with V_{DS}=20 V (right ordinate axis).

In summary we have demonstrated the possibility to produce high performance oxide based bottom gate TFTs replacing the In by Sn in the Ga–Zn–O system, which is an important advantage due to the limited availability of In. The morphological and structural characteristics have been determined, revealing very smooth surfaces, typical for amorphous materials. XPS analysis reveals a segregation of Ga^{3+} and specially of Sn^{4+} at the surface induced by annealing. The device electrical characteristics are drastically improved when the TFTs are subjected to a postannealing treatment to a temperature of 300 °C, without changing the amorphous structure of the multicomponent semiconductor. The annealing treatment controls device characteristics and minimizes the effect of other process parameters. The performances of the *a*-GSZO presented in this letter are comparable and in some cases superior than those of *a*-GIZO TFTs.

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